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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/599,170	09/21/2006	Ryuta Nakanishi	P30744	5285

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EXAMINER	
DUDEK JR, EDWARD J	
ART UNIT	**PAPER NUMBER**
2186	

NOTIFICATION DATE	DELIVERY MODE
12/17/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/599,170	NAKANISHI ET AL.	
	Examiner	Art Unit	
	Edward J. Dudek	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 September 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/21/06, 06/27/07, 03/10/08, 05/29/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to application #10/599170 filed on 21 September 2006.

Claims 1 and 3-18 are pending and have been presented for examination.

Claim 2 has been cancelled.

Drawings

The drawings are objected to because in figure 9 the control unit is referred to as element 38 but paragraph [0095] of the specification refers to the control unit as element 138. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the

examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 16 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 16 contains the limitation "… a change unit operable to change an access order of the selected line in order information indicating an order in which lines are accessed." This limitation is not clear, and does not make sense. For purposes of applying art, the limitation will be interpreted as referring to a cache line replacement strategy where the selected line is selected based on an order in which the lines are accessed.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 18 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 18 is a method claim, and therefore is claiming a process. The claim does not satisfy the machine or transformation test as laid out by the Supreme Court. With regard to the machine test, there are no limitations in the claim that tie the process to another statutory category such as a machine or article of manufacture. With regard to the transformation test, the process claimed does not perform a physical transformation of the underlying subject matter. Since the claim fails the machine or transformation test the claim is non-statutory.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-11, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Afsar (**U.S. Patent #6,401,193**).

As per claims 1 and 18: Afsar discloses a cache memory system comprising: a condition generation unit operable to generate a condition concerning a state of a processor **(see column 6, lines 1-21)**; a judgment unit operable to judge whether or not a current state of the processor satisfies the condition **(see column 8, lines 1-17)**; an address generation unit operable to generate an address to be manipulated **(see column 6, lines 37-55)**; and a manipulation unit operable to manipulate a cache using the address generated by said address generation unit, when said judgment unit judges that the condition is satisfied **(see column 8, lines 18-64)**, wherein said condition generation unit is operable to generate a new condition in the case where said judgment unit judges that the condition is satisfied **(see column 7, lines 49-67)**.

As per claim 3: wherein said condition generation unit is operable to generate a condition concerning a value of a specific register, within the processor **(see column 8, lines 1-16)**.

As per claim 4: wherein the specific register is a program counter **(see column 8, lines 1-16)**.

As per claim 5: wherein said condition generation unit is operable to generate, as the condition, one of memory access within a specific address range and memory access outside of the specific address range **(see column 6, lines 1-21)**.

As per claim 6: wherein said condition generation unit is operable to generate, as the condition, execution of a specific instruction by the processor **(see column 6, lines 1-21)**.

As per claim 7: wherein said condition generation unit is operable to generate the new condition by performing a specific calculation on a current condition **(see column 6, lines 22-36)**.

As per claim 8: wherein said condition generation unit is operable to: generate a memory access address as the condition **(see column 6, lines 1-21)**; and generate the new condition by adding a constant to the current condition in the case where said judgment unit judges that the condition is satisfied **(see column 6, lines 37-55)**.

As per claim 9: wherein the constant is one of: an increment value or decrement value in a post-increment load/store instruction executed by the processor; and a difference value of addresses in two load/store instructions executed by the processor **(see column 6, lines 37-55)**.

As per claim 10: wherein said condition generation unit is operable to generate plural conditions **(see column 7, lines 49-67)**, and said judgment unit is operable to judge whether or not all of the plural conditions are satisfied **(see column 8, lines 1-17)**.

As per claim 11: wherein said condition generation unit is operable to generate plural conditions **(see column 7, lines 49-67)**, and said judgment unit is operable to judge whether or not any of the plural conditions are satisfied **(see column 8, lines 1-17)**.

Claims 1, 3-4, 6, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Shinozaki (**JP 11-167520**).

As per claims 1 and 18: Shinozaki discloses a cache memory system comprising: a condition generation unit operable to generate a condition concerning a state of a processor **(see [0034])**; a judgment unit operable to judge whether or not a current state of the processor satisfies the condition **(see [0029])**; an address generation unit operable to generate an address to be manipulated **(see [0030])**; and a manipulation unit operable to manipulate a cache using the address generated by said address generation unit, when said judgment unit judges that the condition is satisfied **(see [0041])**, wherein said condition generation unit is operable to generate a new condition in the case where said judgment unit judges that the condition is satisfied **(see [0034])**.

As per claim 3: wherein said condition generation unit is operable to generate a condition concerning a value of a specific register, within the processor **(see [0034])**.

As per claim 4: wherein the specific register is a program counter **(see [0034], the program counter typically holds the address of the next instruction)**.

As per claim 6: wherein said condition generation unit is operable to generate, as the condition, execution of a specific instruction by the processor **(see [0042])**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12, and 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Afsar (**U.S. Patent #6,401,193**) in view of well known practices in the art.

As per claim 12: Afsar discloses all the limitations of claim 1 as discussed above. Afsar further discloses wherein said manipulation unit includes: a data judgment unit operable, in the case where said judgment unit judges that the condition is satisfied, to judge whether or not data corresponding to the address generated by said address generation unit is stored in the cache **(see column 8, lines 18-33)** and a transfer unit operable to transfer, from a memory to the selected line, the data corresponding to the address **(see column 8, lines 34-64)**. Afsar fails to disclose a selection unit operable to select a line within the cache memory in the case where it is judged that the data is not stored; a write back unit operable to perform a write back from the selected line when the selected line is valid and dirty; and a registration unit operable to register the address as a tag to the selected line. The system of Afsar involves pre-fetching data to a cache memory so the data is already present when the processor needs the data. Cache memories are relatively small and therefore can only hold a few entries. The data in the cache is cycled in and out throughout the execution of a program. As entries are removed from the cache, the data in the cache line must be written back to main memory if the data has been updated, this is what is known as a write back cache, and Official Notice is hereby taken. Furthermore, when a system is determining if data is present in a cache memory, the tag memory is searched. The tag memory contains addresses to the data that is stored in the cache. When a cache line is updated, the tag associated with the line is also updated, and Official Notice is hereby taken. It would

have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have selected a line for replacement in the cache memory, since space is limited and lines are replaced from time to time, perform a write back of data in the selected line if the data has been updated so that the updated data is not lost, and to register the address of the new data in the tag memory so the data line can be searched when looking for the data in the cache memory.

As per claim 14: Afsar discloses all the limitations of claim 1 as discussed above. Afsar further discloses wherein said manipulation unit includes: a data judgment unit operable, in the case where said judgment unit judges that the condition is satisfied, to judge whether or not data corresponding to the address generated by said address generation unit is stored in the cache **(see column 8, lines 18-33)** and a selection unit operable in the case where it is judged that the data is stored, to select a line, within the cache memory, in which the data is stored **(see column 8, lines 18-30)**. Afsar fails to disclose a write back unit operable to perform a write back from the selected line when the selected line is valid and dirty. There are two methods for ensuring that data that is written to a cache memory is updated in main memory. A write though method which involves updating data in main memory whenever the data in the cache line is updated and a write-back method that involves updating data in the main memory whenever the data is evicted from the cache memory. Both techniques have their advantages. A write thought method puts more traffic on the memory bus as data is constantly being sent to the main memory to update any data lines that have been written to, but allows faster eviction as the data can just be cast out without having to first wait for the data in

main memory to be updated. A write back technique reduces the amount of traffic on the memory bus, but requires a wait time when evicting the data since the data in the main memory must first be updated so that any changes made are not lost. Official Notice of this is hereby taken. "When there is a design need for market pressure to solve a problem and there are a finite number if identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *KSR*, 82 USPQ2d at 1397. It would have been obvious to try each of theses implementations to take advantage of the benefits each technique offers in order to achieve the best performance.

As per claim 15: Afsar discloses all the limitations of claim 1 as discussed above. Afsar further discloses wherein said manipulation unit includes: a data judgment unit operable, in the case where said judgment unit judges that the condition is satisfied, to judge whether or not data corresponding to the address generated by said address generation unit is stored in the cache **(see column 8, lines 18-33)** and a selection unit operable in the case where it is judged that the data is stored, to select a line, within the cache memory, in which the data is stored **(see column 8, lines 18-30)**. Afsar fails to disclose an invalidation unit operable to invalidate the selected line. Whenever data that is held in a cache memory is updated somewhere else in the system, and the data line no longer contains valid data, the data line is invalidated, this is a common memory coherence technique to make sure only the current version of data is used, and Official Notice is hereby taken. It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have a data invalidation unit in the

system of Afsar to invalidate data in the cache when that data line is updated somewhere else and is no longer valid to make sure any programs that use that data only use the current version of the data.

As per claim 16: Afsar discloses all the limitations of claim 1 as discussed above. Afsar further discloses wherein said manipulation unit includes: a data judgment unit operable, in the case where said judgment unit judges that the condition is satisfied, to judge whether or not data corresponding to the address generated by said address generation unit is stored in the cache **(see column 8, lines 18-33)** and a selection unit operable in the case where it is judged that the data is stored, to select a line, within the cache memory, in which the data is stored **(see column 8, lines 18-30)**. Afsar fails to disclose a change unit operable to change an access order of the selected line in order information indicating an order in which lines are accessed. Cache replacement techniques are well known in the art. Selecting a replacement line based on the order in which the data is accessed allows older data to be replaced before newer data is, thereby keeping more useful data in the cache, and Official Notice is hereby taken. It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have used an access order replacement technique in the system of Afsar to keep the most relevant data in the cache and to replace the older data.

As per claim 17: Afsar discloses all the limitations of claim 12 as discussed above. Afsar further discloses wherein said condition generation unit is operable to generate a memory address as the condition **(see column 6, lines 1-21)**. Afsar fails to

disclose said manipulation unit further includes an adjustment unit operable, in the case where the memory address generated by said condition generation unit indicated a point midway through a line, to generate an address by adjusting so that one of a starting point of the line, a starting point of a next line, and a starting point of an immediately preceding line is indicated. When data is stored in an cache, the address of the line is maintained in a cache tag. Only a subset of the address is needed since each cache line stores a specific amount of data, the least significant bits are not needed to identify the line. This means that the addresses must occur in specific intervals depending on the design of the system (e.g. 16K, 32K, 64K, etc.). Official Notice of this is hereby taken. Therefore, if an address is generated that falls between these boundaries, the address will have to be adjusted to coincide with the size of the address that is maintained in the cache tag. It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by Afsar to modify any predicted addresses to coincide with the cache line boundaries and to adhere to the requirements of the cache tag array.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Afsar (**U.S. Patent #6,401,193**) in view of Yamada (**JP 07-084879**) and well known practices in the art.

As per claim 13: Afsar discloses all the limitations of claim 1 as discussed above. Afsar further discloses wherein said manipulation unit includes: a data judgment unit operable, in the case where said judgment unit judges that the condition is satisfied, to

judge whether or not data corresponding to the address generated by said address generation unit is stored in the cache **(see column 8, lines 18-33)** and a selection unit operable in the case where it is judged that the data is stored, to select a line, within the cache memory, in which the data is stored **(see column 8, lines 18-30)**. Afsar fails to disclose a write back unit operable to perform a write back from the selected line when the selected line is valid and dirty and a registration unit operable to register the generated address as a tag, to the selected line, without transferring data from a memory to the selected line. There are two methods for ensuring that data that is written to a cache memory is updated in main memory. A write though method which involves updating data in main memory whenever the data in the cache line is updated and a write-back method that involves updating data in the main memory whenever the data is evicted from the cache memory. Both techniques have their advantages. A write thought method puts more traffic on the memory bus as data is constantly being sent to the main memory to update any data lines that have been written to, but allows faster eviction as the data can just be cast out without having to first wait for the data in main memory to be updated. A write back technique reduces the amount of traffic on the memory bus, but requires a wait time when evicting the data since the data in the main memory must first be updated so that any changes made are not lost. Official Notice of this is hereby taken. "When there is a design need for market pressure to solve a problem and there are a finite number if identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *KSR*, 82 USPQ2d at 1397. It would have been obvious to try each of

theses implementations to take advantage of the benefits each technique offers in order to achieve the best performance. The combination still fails to disclose a registration unit operable to register the generated address as a tag, to the selected line, without transferring data from a memory to the selected line. Yamada discloses a technique of loading an address into a cache memory without transferring the data associated with the address from main memory to the cache because the data is just going to be over written **(see [0035]-[0036])**. Since the data is just going to be over written, there is no need to load the data from main memory. This will subsequently reduce the load on the bus **(see [0036])**. It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the combination to allow registering of a cache line without transferring the data from main memory when the data is just going to be over written anyway, thereby reducing the load on the bus, as taught by Yamada.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edward J. Dudek whose telephone number is 571-270-1030. The examiner can normally be reached on Mon thru Thur 7:30-5:00pm Sec. Fri 7:30-4 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Pierre-Michel Bataille/
Primary Examiner, Art Unit 2186

/E. J. D./
Examiner, Art Unit 2186
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